DESCRIPTION

RADIO WAVE RECEIVER, RADIO-CONTROLLED TIMEPIECE AND TUNING CAPACITANCE SETTING METHOD

Technical Field

The present invention relates to a radio wave receiver, a radio-controlled timepiece and a tuning capacitance setting method.

Background Art

At the present day, there is known a so-called radio-controlled timepiece which receives long-wave standard time radio waves with time data, i.e., a time code transmitted in respective countries (e.g., Germany, United Kingdom, Japan and others) and corrects time data of a clocking circuit based on the received radio waves.

Meanwhile, when radio waves are received by using, e.g., a bar antenna, there is used a tuning circuit which receives radio waves by causing an inductance of the antenna, a capacitor and the like to be resonant with radio waves having a desired frequency. In such a tuning circuit, tuning with radio waves having a desired frequency is effected by changing a capacity to be connected to the antenna.

It is general that a conventional radio-controlled timepiece comprises a radio wave receiving circuit including such a tuning circuit. As one of such

circuits, there is known a radio wave receiving circuit which performs tuning with long-wave standard time radio waves by using a method to attach a plurality of chip capacitors.

That is, at the time of industrial assembly, an inductance of an antenna is measured, and chip capacitors whose capacitances are not more than a desired capacitance are first attached by soldering. Then, a resonance frequency is measured, an insufficient capacitance is calculated, and a chip capacitor whose capacitance is slightly smaller than the insufficient capacitance is further attached by soldering. Furthermore, operations to measure the resonance frequency and adjust the tuning capacitance are repeatedly carried out according to needs, and adjustment is effected in such a manner that the radio wave receiving circuit performs optimum tuning with respect to the long-wave standard time radio waves.

Moreover, Japanese Patent Application KOKAI Publication No. 6-125280 discloses a radio wave receiving circuit which comprises two capacitors included in a tuning circuit in parallel and can select a resonance frequency by switching a connection of one of the capacitors based on ON/OFF of a switch and changing a tuning capacitance. However, this is used to switch a resonance frequency to be selected, but it is not intended to change a capacitance in order to

tune with radio waves having a desired frequency.

The method for attaching the plurality of chip capacitors requires adjustment of a tuning capacitance when assembling a product, but operations to measure a resonance frequency and attach capacitors must be repeatedly carried out in that adjustment. Therefore, the number of working steps, a working time, a cost and others are taken. Additionally, capacitors, a switch element which switches the capacitors and others are required in accordance with the number of frequencies of radio waves to be received. Therefore, when receiving a plurality of radio waves, applying the technique disclosed in Japanese Patent Application KOKAI Publication No. 6-125280 increases the number of components or a substrate area, and hence a reduction in size of the circuit is difficult.

Further, if tuning adjustment is performed only in a circuit substrate for tuning having an antenna and capacitors mounted thereon and then the adjusted circuit substrate is set in a radio-controlled timepiece and connected with a timepiece circuit substrate, a resonance frequency deviates due to an IC other than the tuning circuit substrate, an input capacitance of the timepiece circuit substrate or the like. Therefore, when trying to perform complete adjustment of the tuning capacitance, tuning adjustment must be again performed in the entire radio-controlled

timepiece.

Disclosure of Invention

According to an embodiment of the present invention, there is provided a radio wave receiver which can be automatically set in a tuning state optimum relative to radio waves having a predetermined frequency, a radio-controlled timepiece and a tuning capacitance setting method.

According to another embodiment of the present invention, there is provided a radio wave receiver for receiving radio waves having a predetermined frequency, the receiver comprises an antenna, an variable capacitor connected to the antenna, a memory, and a controller which determines an optimum capacitance of the variable capacitor with which the radio wave receiver is in a predetermined reception state and writes optimum capacitance data into the memory and, controls the variable capacitor based on the optimum capacitance data.

Additional objects and advantages of the present invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the present invention.

The objects and advantages of the present invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed

out hereinafter.

Brief Description of Drawings

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the present invention and, together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the present invention in which:

FIG. 1 is a view showing a waveform of long-wave standard time radio waves;

FIG. 2 is a block diagram showing an internal structure of a radio-controlled timepiece according to an embodiment of the present invention;

FIG. 3 is a circuit block diagram of a radio wave receiver depicted in FIG. 2;

FIG. 4 is a circuit configuration diagram of a capacitor array depicted in FIG. 3;

FIG. 5 is a view showing a data configuration of a set value data table depicted in FIG. 3;

FIG. 6 is a flowchart showing an operation of a control circuit in a tuning mode according to the embodiment of the present invention;

FIG. 7 is a flowchart showing an operation of the control circuit in a receiving mode according to the embodiment of the present invention;

FIG. 8 is a relationship view of a reception level

of a radio wave signal and a tuning capacitance according to the embodiment of the present invention; and

FIG. 9 is a circuit configuration diagram of a capacitor array when using a variable capacitance diode.

Best Mode of Carrying Out the Invention

An embodiment according to the present invention will now be described hereinafter with an illustrated example. Although a description will be given as to an example in which a radio wave receiver according to the present invention is applied to a radio-controlled timepiece in each embodiment, the example to which the present invention can be applied is not restricted thereto as long as it is an apparatus used to receive radio waves.

In Japan, long-wave standard time radio waves of 40 kHz and 60 kHz subjected to amplitude modulation with a time code having such a format as shown in FIG. 1 are transmitted from two transmitting stations (Fukushima prefecture and Saga prefecture). According to FIG. 1, the time code is transmitted in a frame of one cycle composed of 60 seconds every time a digit of a minute of a correct time is updated, i.e., every one minute.

FIG. 2 is a circuit configuration diagram of a radio-controlled timepiece 1. The timepiece 1

comprises a CPU (Central Processing Unit) 101, an input device 102, a display device 103, an RAM (Random Access Memory) 104, an ROM (Read Only Memory) 105, a reception controller 106, a time code generator 107, a clocking circuit 108 and an oscillation circuit 109. The respective portions except the oscillation circuit 109 are connected with each other through a bus 110. The oscillation circuit 109 is connected to the clocking circuit 108.

The CPU 101 reads various kinds of programs stored in the ROM 105 and develops them in the RAM 104 in accordance with a predetermined timing or an operation signal or the like input from the input device 102, and performs instruction or data transfer to each function portion based on the programs.

The CPU 101 executes receiving processing of long-wave standard time radio waves by controlling the reception controller 106 every, e.g., predetermined time, corrects current time data counted in the clocking circuit 108 based on a standard time code input from the time code generator 107, outputs a display signal based on the corrected current time data to the display device 103, and performs various controls such as updating of a displayed time. Moreover, the CPU 101 outputs a signal indicative of one of two operating modes, i.e., a tuning mode and a receiving mode to the radio wave receiver 200.

The input device 102 comprises switches or the like which cause the radio-controlled timepiece 1 to execute various functions. Additionally, when these switches are operated, operation signals of corresponding switches are output to the CPU 101.

The display device 103 comprises a small liquid crystal display or the like, and digitally displays data from the CPU 101, e.g., current time data or the like obtained by the clocking circuit 108.

The RAM 104 is used to store data processed by the CPU 101 and output stored data to the CPU 101 under control of the CPU 101. The ROM 105 mainly stores a system program concerning the radio-controlled timepiece 1 and an application program.

The reception controller 106 comprises the radio wave receiver 200. The radio wave receiver 200 takes out a corresponding frequency signal by cutting an unnecessary frequency component of the long-wave standard time radio waves, converts the frequency signal into a corresponding electrical signal, and outputs it.

The time code generator 107 generates a standard time code including data required for a clock function such as a standard time code, an integration code, a day code and the like based on the signal output from the radio wave receiver 200, and outputs it to the CPU 101.

The clocking circuit 108 counts signals input from the oscillation circuit 109, and obtains the current time data and the like. Then, it outputs the current time data to the CPU 101. The oscillation circuit 109 is a circuit which constantly outputs signals with a fixed frequency.

FIG. 3 is a circuit block diagram of the radio wave receiver 200 in this embodiment. The radio wave receiver 200 comprises, e.g., an antenna ANT, a capacitor array 201, a front-end circuit 202, a detection-and-rectifying circuit 203, a waveform shaping circuit 204, a reception level detection circuit 205, a control circuit 206, and a memory 207.

The antenna ANT can receive the long-wave standard time radio waves, and it is constituted of, e.g., a bar antenna. The receive radio waves are input to the capacitor array 201.

FIG. 4 shows a circuit configuration of the capacitor array 201. The capacitor array 201 includes capacitors C1 to Cn (n is an integer not less than 2) and transistors T1 to Tn provided inside an IC (integrated circuit). Each of the capacitors C1 to Cn and each of the transistors T1 to Tn are connected in series. The series connections of the capacitor C1 (C2 to Cn) and the transistor T1 (T2 to Tn) are connected with each other in parallel.

Furthermore, the capacitor array 201 includes

connection terminals J1 and J2 so that external capacitors Cex1 and Cex2 attached to the outside of the IC can be connected. The external capacitors Cex1 and Cex2 are respectively connected with transistors Tex1 and Tex2 in series, and further connected to the capacitors C1 to Cn in parallel. The external capacitors Cex1 and Cex2 are capacitors which have relatively large capacitances as compared with, e.g., those of the capacitors C1 to Cn, and they are added according to circumstances.

The capacitors C1 to Cn are combined with each other by the switching operations of the corresponding transistors T1 and Tn, and a capacitance of the entire capacitor array 201 is controlled. In the later-described tuning mode, since the transistors T1 to Tn are sequentially switched so as to increase a capacitance of the entire capacitor array 201, the capacitors C1 to Cn are arranged in a predetermined order, e.g., an ascending order of capacitances.

A capacitance selection signal S1 output from the control circuit 206 is input to a decoder 300. The decoder 300 decodes the capacitance selection signal S1, and outputs switching data used to control ON/OFF of each transistor. Switching data D1 to Dn, Dex1 and Dex2 output from the decoder 300 are respectively input to gates of the transistors T1 to Tn, Tex1 and Tex2.

For example, when the switching data D1 is "1",

the transistor T1 is turned on, and the capacitor C1 is connected to the antenna ANT in parallel. When the switching data D1 is "0", the transistor T1 is turned off, and the capacitor C1 is electrically disconnected from the antenna ANT. The same operation is carried out with respect to the other transistors.

The decoder 300 is not restricted to the above-described structure as long as it is a circuit (e.g., a multiplexer or a ring counter) which outputs a signal which can control ON/OFF of each transistor in accordance with the capacitance selection signal S1.

A tuning frequency is controlled based on an inductance of the antenna ANT and a capacitance of the capacitor connected to the antenna ANT in parallel, and radio waves received by the antenna ANT are converted into an electrical signal and output as a signal S2.

The signal S2 and a signal S5 are input to the front-end circuit 202. The front-end circuit 202 applies predetermined signal processing to the signal S2, and outputs the processed signal as a signal S3.

When the radio wave receiver 200 is formed as a straight type, the front-end circuit 202 includes an amplification circuit which amplifies the signal S2, a filter or the like. When the radio wave receiver 200 is constituted as a super heterodyne type, the front-end circuit 202 includes, e.g., an oscillation circuit which generates a signal having a local

oscillatory frequency, and a frequency conversion circuit which generates an intermediate frequency signal by combining a signal generated by the oscillatory circuit with the signal S2.

The front-end circuit 202 performs adjustment (AGC or the like) of an amplification of the amplification circuit included in the circuit based on the signal S5 which is an AGC feedback voltage in such a manner that a signal level of the signal S3 to be output is changed to an optimum level.

The signal S3 is input to the detection-and-rectifying circuit 203, and this circuit 203 detects a base band signal from the signal S3. The detection-and-rectifying circuit 203 outputs the detected base band signal as a signal S4. The detection-and-rectifying circuit 203 outputs the signal S5 to the front-end circuit 202 and the reception level detection circuit 205 in accordance with a signal level of the signal S3.

The signal S4 is input to the waveform shaping circuit 204, and this circuit 204 performs waveform shaping of the signal S4 so as to obtain a signal optimum for the time code generator 107 and outputs a result as a signal Sd. The signal S5 is input to the reception level detection circuit 205, and this circuit 205 performs processing by, e.g., amplifying the signal S5 and outputs a result as a reception level signal S6.

The reception level signal S6 and a signal S0 from the CPU 101 are input to the control circuit 206. The signal S0 is a signal indicative of one of the tuning mode and the receiving mode. When the signal S0 is indicative of the tuning mode, the control circuit 206 outputs the capacitance selection signal S1 used to control ON/OFF of the transistors T1 to Tn, Tex1 and Tex2 in the capacitor array 201. Combinations of ON/OFF of the transistors T1 to Tn, Tex1 and Tex2 when indicating optimum tuning with the received radio waves are stored in the memory 207 based on the reception level signal S6.

When the signal S0 is indicative of the receiving mode, the control circuit 206 reads a set value corresponding to a frequency of the received radio waves from the memory 207, and outputs the set value as the capacitance selection signal S1 to the capacitor array 201. A detailed flow of operations in the tuning mode and the receiving mode will be described later with reference to a flowchart.

The control circuit 206 includes a set value memory 2061 and a reception level memory 2062. Each memory is constituted of a temporary memory such as a RAM.

The set value output from the control circuit 206 is stored in the memory 207. The memory 207 is constituted of a nonvolatile memory such as an EEPROM

(Electrically Erasable Programmable Read-Only Memory) which can read/write data, and stores a set value data table 2071 or the like therein.

FIG. 5 is a view showing an example of the set value data table 2071. In the set value data table 2071 are stored frequencies of the received radio waves and set values of the capacitance selection signal S1 in association with each other.

Giving a concrete description, in regard to the switching data D1 to Dn, Dex1 and Dex2 output from the decoder 300, assuming that n = 6, there can be obtained eight sets of switching data D1 to D6, Dex1 and Dex2, and the eight sets of data are used to control ON/OFF of the eight transistors T1 to T6, Tex1 and Tex2.

For example, in the receiving mode, when the set value of the capacitance selection signal S1 output from the control circuit 206 is "14H", this value is decoded as "00010100" by the decoder 300. The switching data has values corresponding to respective bits in the decoded value. For example, the switching data D1 to D3, D5, Dex1 and Dex2 are "0", and the switching data D4 and D6 are "1". They are input to the gates of the respective transistors T1 to T6, Tex1 and Tex2. Then, since the transistors T4 and T6 are turned on, the capacitors C4 and C6 are connected to the antenna ANT in parallel.

For example, in the receiving mode, when trying

tuning to the radio waves having a second frequency, the control circuit 206 reads a set value "30H" corresponding to the second frequency from the set value data table 2071. Then, it outputs the set value as the capacitance selection signal S1 to the decoder 300 of the capacitor array 201.

In this case, the value of the capacitance signal S1 is decoded as "00110000" by the decoder 300. For example, the switching data D1, D2, D5, D6, Dex1 and Dex2 are input as "0" and the switching data D3 and D4 are input as "1" to the gates of the respective transistors. Then, the transistors T3 and T4 are turned on, and the capacitors C3 and C4 are connected to the antenna ANT in parallel.

Each set value is set in the tuning mode, and stored in the set value data table 2071. The set values differ from each other depending on each radio-controlled timepiece based on characteristics of the radio wave receiver 200 or affections of any other circuits.

A description will now be given as to a method for setting a tuning capacitance with respect to a predetermined frequency of the capacitor array 201. FIG. 6 is a flowchart illustrating a flow of the operation of the control circuit 206 in the tuning mode. When the signal S0 indicative of the tuning mode is input to the control circuit 206 from the CPU 101,

the operation in the tuning mode starts.

The tuning mode is carried out, e.g., before factory shipment after the radio wave receiver 200 is assembled as an internal circuit of the radio-controlled timepiece instead of an elemental unit formed of only the radio wave receiver 200.

The control circuit 206 outputs a capacitance selection signal S1 instructing to turn off all the transistors T1 to Tn, Tex1 and Tex2 included in the capacitor array 201 (step A1). The control circuit 206 stores a set value of the capacitance selection signal S1 output at step A1 in the set value memory 2061 (step A2).

The control circuit 206 stores a value of the reception level signal S6 in the reception level memory 2062 (step A3), changes the set value of the capacitance selection signal S1 so as to increase the tuning capacitance of the capacitor array 201 by one level, and outputs a result (step A4).

The control circuit 206 compares the value of the reception level signal S6 with the value stored in the reception level memory 2062 (step A5). When the value indicated by the reception level signal S6 is larger than the stored value (step A6; Yes), the operation is repeated from step A2.

When the value indicated by the reception level signal S6 is smaller than the stored value (step A6;

No), the control circuit 206 stores in the set value data table 2071 the data stored in the set value memory 2061 (step A7). At this step, the set value is stored in association with the frequency of the received radio waves. Then, the tuning mode is terminated.

A comparison judgment of the reception level at step A6 will now be described in details. FIG. 8 is a view showing a relationship between the tuning capacitance of the capacitor array 201 and the reception level indicated by the reception level signal S6.

For example, a reception level X for a tuning capacitance C of the capacitor array 201 is stored in the reception level memory 2062. The control circuit 206 outputs the capacitance selection signal S1 so as to increase the tuning capacitance of the capacitor array 201 by one level (corresponding to step A4) and the tuning capacitance is changed to C'. The reception level signal S6 at this moment indicates a reception level X'. Since the reception level X < the reception level X' is achieved, the set value of the capacitance selection signal S1 is stored in the set value memory 2061 (corresponding to step A2). The reception level X' is stored in the reception level memory 2062 (corresponding to step A3).

Subsequently, the control circuit 206 again outputs the capacitance selection signal S1 so as to

increase the tuning capacitance of the capacitor array 201 by one level (corresponding to step A4) and the tuning capacitance is changed to C". The reception level signal S6 at this moment is indicative of the reception level X, the reception level X < the reception level X' is achieved. That is, the set value of the previously output capacitance selection signal S1 derived the reception level higher than that of the set value of the currently output capacitance selection signal S1.

Therefore, it is determined that the combination of ON/OFF of the transistors T1 to Tn, Tex1 and Tex2 indicated by data stored in the set value memory 2061 corresponds to a state that optimum tuning for the received radio waves is performed, and the data stored in the set value memory 2061 is stored in a set value data table 2071 (corresponding to step A7).

FIG. 7 is a flowchart illustrating a flow of an operation of the control circuit 206 in the receiving mode. When the signal S0 indicative of the receiving mode is input to the control circuit 206 from the CPU 101, an operation in the receiving mode is started.

The control circuit 206 reads a set value corresponding to a frequency of received radio waves from the set value data table 2071 (step B1), and outputs the read set value as a capacitance selection signal S1 to the capacitor array 201 (step B2).

Upon receiving the capacitance selection signal S1, the capacitor array 201 decodes it in the decoder 300, and outputs switching data to a gate of each transistor. As a result, a capacitor to be connected to the antenna ANT in parallel is determined, and a tuning capacitance optimum for the received radio waves can be obtained.

As described above, the tuning capacitance of the capacitor array 201 is increased in increments of one level (capacitance is enlarged) in the tuning mode, and a value of the reception level signal S6 at that moment is compared with a value of the previous reception level signal S6. If a value of the previous reception level signal S6 is larger, a set value of the capacitance selection signal S1 indicative of a combination of the previous capacitor connection of the capacitor array 201 is stored in the memory 207.

As a result, a combination of the capacitor connection used to perform optimum tuning with respect to the received radio waves (tuning capacitance) can be readily known. Further, since set values of the plurality of capacitance selection signals S1 can be stored in the memory 207, a radio wave receiver capable of receiving radio waves having a plurality of frequencies can be realized.

Furthermore, in the receiving mode, when a set value corresponding to a frequency of the radio waves to be received is output to the capacitor array 201 as

the capacitance selection signal S1, it is possible to readily set a tuning capacitance indicative of optimum tuning with respect to the received radio waves.

According to the radio wave receiver of the embodiment, since a capacitance which should be connected in order to cause a reception state of radio waves having a predetermined frequency to enter a predetermined receiving state is determined and stored, tuning with the radio waves having the predetermined frequency can be automatically effected.

Although the embodiment to which the present invention is applied has been described above, the present invention is not limited to the foregoing embodiment, and various modifications can be of course added without departing from the scope of the invention.

For example, as shown in FIG. 4, the capacitor array 201 is constituted by connecting in parallel the plurality of transistors connected in series with the plurality of capacitors, and a tuning capacitance can be varied by controlling ON/OFF of the transistors by using switching data output from the decoder 300. However, the tuning capacitance may be varied by using a variable capacitance diode.

FIG. 9 is a circuit configuration diagram of a capacitor array 800 when using a variable capacitance diode D. The capacitor array 800 is constituted of,

e.g., a variable capacitance diode D, capacitors C11 and C12, a resistor R, and a D/A converter 801.

A capacitance selection signal S1 output from the control circuit 206 is input to the D/A converter 801. Moreover, D/A conversion is carried out based on a set value of the capacitance selection signal S1, and a signal having a predetermined voltage level is output. A capacitance of the variable capacitance diode D is varied in accordance with a voltage level of a signal output from the D/A converter 801. As a result, a tuning capacitance of the capacitance array 800 is changed, and it is possible to set a tuning frequency used to perform optimum tuning with respect to received radio waves.

Additionally, although the description has been given as to the case in which the tuning mode and the receiving mode are carried out as different modes, these two modes may be performed simultaneously as one mode. For example, the tuning mode is effected before performing the receiving mode, and a set value indicative of optimum tuning relative to received radio waves is obtained. Thereafter, the receiving mode is performed, thereby realizing the radio wave receiver effecting tuning always optimum with respect to received radio waves.